Digital electronics (extended candidates)

Mark Scheme 1

Level	IGCSE
Subject	Physics
ExamBoard	CIE
Topic	Electricity and Magnetism
Sub-Topic	Digital electronics (extended candidates)
Paper Type	(Extended) Theory Paper
Booklet	Mark Scheme 1

Time Allowed: **58 minutes**

Score: **/48**

Percentage: **/100**

Question	Answer	Mark
1(a)(i)	<u>Light emitting</u> diode OR LED	**B1**
(a)(ii)		**B1**
(b)	column C column E 0 0 0 1 0 0 0 1 0 0 0 1 1 1 1 1	**B3**
(c)	Replace the OR gate with an AND gate	**B1**
		Total: 6

2 **a(i)** AND (gate) B1

a(ii) 0 0 1 B2
1 0 0
0 1 0
1 1 0

(b)

A	B	**C**	**D**	**E**	F
1	**1**	**0**	**1**	**1**	**1**

B3

[Total: 6]

3 **(a** output of A: 1, 1, 0, 0 c.a.o. [1]
output of B: 0, 1, 0, 0 e.c.f. from candidate's output of A [1]

(b) dark AND hot owtte
note: must be consistent with answer to **(a)** [1]

(c) B cannot provide enough power / current for lamp, or equivalent
OR allows remote lamp [2]
note: statement of function of a relay without reference to context gains 1 mark

a(ii)

4 **(a)** **(i)** OR (gate)   B1

   (ii)   1 input and 1 output labelled <u>with words</u>   B1

   (iii) correct symbol

                                                                                            B1

   (b) **(**   needle not deflected   B1

       (ii) needle not deflected   B1

       (iii) needle deflected either way   B1

                                                                                    [Total: 6]

5 **(a** **(i)** NAND   B1

       (ii) output and one input correctly labelled   B1

   (b) rectangle with longitudinal line in middle third, no input or output wire required   B1

   (c) **(i)** temperature (decreases)   B1

       (ii) correctly relates change of resistance to change of temperature   B1
           voltage of mid-point (of potential divider)/left of LED increases OR higher V across
           thermistor   B1
           current flows through/enough V to light LED   B1

   (d) $1/R_p = 1/R_1 + 1/R_2$ or $(R_p) = R_1R_2/(R_1 + R_2)$ C1
        $(R = 1/(1/4 - 1/6) =) 12\ \Omega$ A1

                                                                                    [Total: 9]

6 **(a)** row 1   0   0   accept low / off   B1

  row 2   0   1   accept low / off and high / on   B1

  row 3   1   1   accept high / on   B1

  (b) 2 wires to flat (input) side, 1 wire from curved (output) side
  do not accept pointed curved side or small circle   B1

  (c) NOT gate connected to output of AND gate
  accept labelled boxes for gates
  do not allow any extra gates or inputs   M1

  NOT gate correct way round

  A1

  [Total: 6]

7 **(a)** in order downwards: 1 1 1 0 c.a.o.   B1

  (b)   1 AND 0 (e.c.f. from **(b)(i)**)   B

  (ii)   NOT (gate) (**allow** NOR (gate))   B1

  (c) R = 1 AND S = 0 (e.c.f. from **(b)(i)**)   B
  T = 1   B1   [5]

8 **(a)** **(i)** AND gate   B1

      (ii) correct symbol must have 2 inputs, 1 output
           concave input side, somewhat pointed on output side with small circle   B1   [2]

  (b) **(** HIGH / 1   B

      (ii) HIGH / 1   B   [2]

  (c) transistor circled   B1   [1]

[Total: 5]